Application Note **MSAN-163**

Multitrunk System Synchronizer

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Contents

Introduction

Digital telecommunication networks are synchronous in nature. Consequently, the equipment connected to a digital network has to be synchronized to it in some manner. Synchronous operation is generally achieved by phase-locking the equipment's system timing to a clock extracted from an incoming digital trunk; often designated as the primary reference source by the network provider. The synchronizer or phase-lock loop (PLL) has to be able to phase lock to the extracted clock and at the same time generate very stable system timing. Short term variations in the frequency and other perturbations in the signal, such as jitter, have to be filtered out to meet network jitter transfer specifications. In addition, when the primary reference source degrades in quality, the synchronizer should have the capability to switch to an alternate reference source.

This application note provides designers with information (which is additional to the MT9042B data sheet) on implementing the MT9042B Multitrunk System Synchronizer in a telecommunications network. The sections covered include reference switching, a detailed example on MTIE and phase slope, network specifications and how they relate to the MT9042B, common MT9042B questions and answers and an application circuit for extending the number of reference inputs on the MT9042B.

Reference Switching

One of the main features of the MT9042B is its ability to perform input reference switching without any significant change in the output phase. This feature enables systems to meet the AT&T TR62411 Maximum Time Interval Error (MTIE) requirements when switching between input references of the same frequency which are different in phase.

AT&T TR62411 recommends that switching from the primary reference source to a secondary reference source (reference switching) be minimized, and not take place until specific reference degradations occur. These reference degradations include:

- A complete loss of signal for 100ms or more.
- Bit error ratios worse than 0.001 for durations of 2.5 seconds or more.
- Phase hits of 1us duration exceeding 61us/s.
- Jitter exceeding the jitter tolerance requirements.

TR62411 also recommends that to prevent too many reference switches in cases when the primary reference source is marginally degraded, the minimum time spent in the secondary reference position should be 10 seconds.

Minimizing switching (from PRI to SEC) in the MT9042B can be realized by first entering Holdover Mode for a predetermined maximum time (guard time). If the degraded signal returns to normal before the expiry of the guard time (e.g., 2.5 seconds), then the MT9042B is returned to its Normal Mode (with no reference switch taking place). Otherwise, the reference input may be changed from Primary to Secondary. Refer to the MT9042B data sheet for information on using the guard time circuit.

TR62411 specifies that for reference switching as well as changes in clock mode (i.e., between Normal Mode and Holdover Mode), MTIE must not exceed 1000ns, and phase slope must not exceed 81ns per 1.326ms (7.6ns/125us). The MT9042B meets these requirements.

TIE, MTIE and Phase Slope Example

Although numerous definitions (see MT9042B data sheet) are given for Time Interval Error (TIE), Maximum Time Interval Error (MTIE) and phase slope, they can best be described with an example.

Consider the TIE and phase slope Example Data shown in Table 1. Note that this data is for illustration purposes only, and is not fabricated from any actual device. In this example, the time interval is measured between an 8kHz output frame pulse and an ideal 8kHz frame pulse. Twenty-one samples are taken, one every 1.326ms. The phase slope is calculated by dividing the phase movement between successive samples, by the sampling interval of 1.326ms.

Measurement Number	Time (ms)	TIE (ns)	Phase Slope (ns/1.326ms)
0	0	200	
1	1.326	160	-40
2	2.652	103	-57
3	3.978	42	-61
4	5.304	-11	-53
5	6.630	-50	-39
6	7.956	-72	-22
7	9.282	-77	-5
8	10.61	-68	+9
9	11.93	-50	+18
10	13.26	-28	+22
11	14.59	-6	+22
12	15.91	12	+18
13	17.24	23	+11
14	18.56	28	+5
15	19.89	27	-1
16	21.11	22	-5
17	22.54	15	-7
18	23.87	6	-9
19	25.19	-1	-7
20	26.52	-6	-5

Table 1- TIE and Phase Slope Example Data

Figure 1 shows the time domain plot or oscilloscope view of the example data of Table 1.

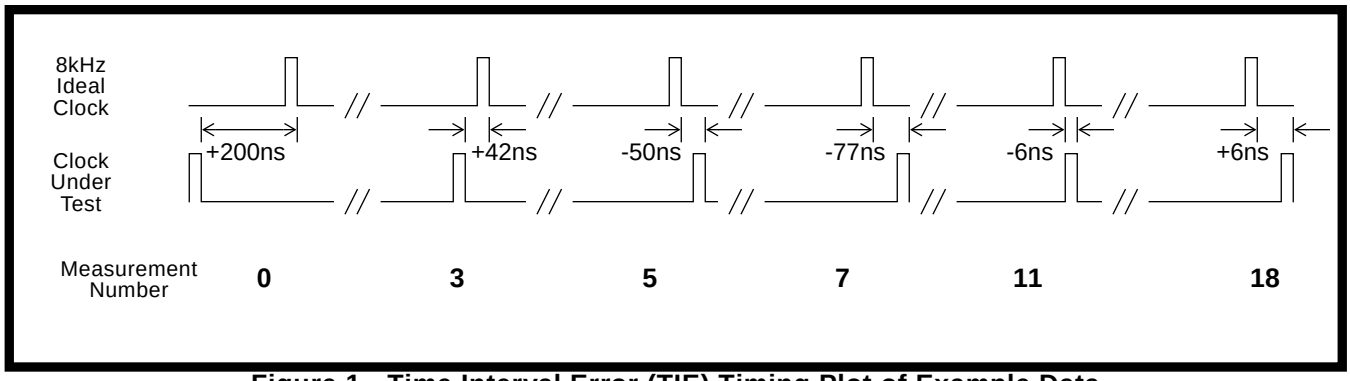

Figure 1 - Time Interval Error (TIE) Timing Plot of Example Data

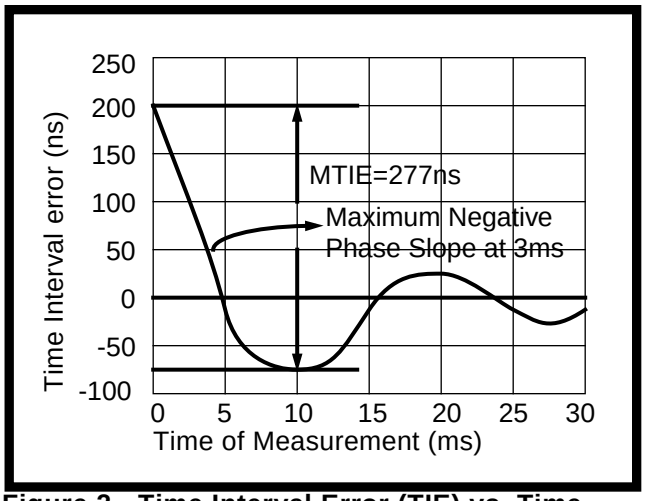

Figure 2 - Time Interval Error (TIE) vs. Time

Figure 2 shows the example data plotted as Time Interval Error (TIE) vs. time of measurement along with the Maximum TIE (MTIE).

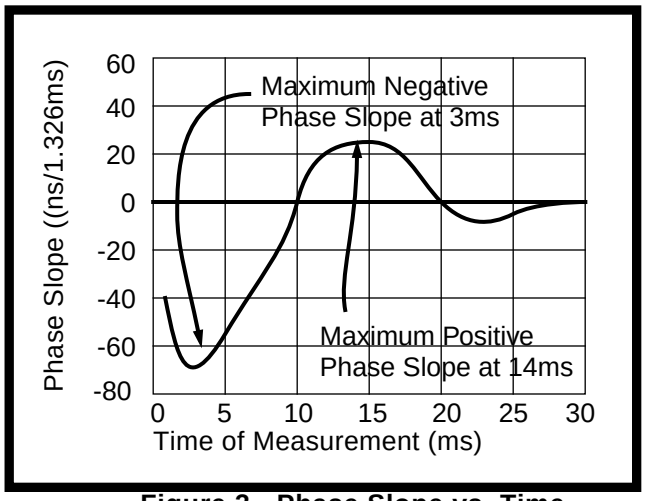

Figure 3 - Phase Slope vs. Time

Figure 3 shows the example data plotted as phase slope vs. time of measurement along with the Maximum phase slope.

Using the test data in Table 1, MTIE is determined as follows.

$$MTIE(S) = TIEmax(t) - TIEmin(t)$$

$$MTIE(30ms) = 200ms(0ms) - 77ms(9.282ms)$$

$$MTIE(30ms) = 277ms$$

Using the test data in Table 1, maximum phase slope is determined directly from the test data.

$$MaxPhaseSlope = 61ns/1.326ms$$

MT9042B and Network Specifications

This section compares the MT9042B with North American AT&T TR62411 specifications and European ETSI ETS 300 011 and ITU-T I.431 specifications. The specifications which are applicable to a synchronizer including intrinsic jitter, jitter tolerance, jitter transfer, frequency accuracy, holdover accuracy, capture range, Maximum Time Interval error (MTIE) and phase slope are all considered.

AT&T Intrinsic Jitter - the MT9042B meets the AT&T TR62411 intrinsic jitter requirements as shown in Table 2.

Filter	AT&T Requirement (UIpp) (maximum)	MT9042B (C1.5o) (UIpp) (maximum)
10Hz-8kHz	0.020	0.005
10Hz-40kHz	0.025	0.010
8kHz-40kHz	0.025	0.010
None	0.050	0.030

Table 2 - AT&T Intrinsic Jitter

AT&T Jitter Tolerance - the MT9042B meets the AT&T TR62411 jitter tolerance requirements for T1 (1.544MHz) frequency inputs as shown in Figure 4.

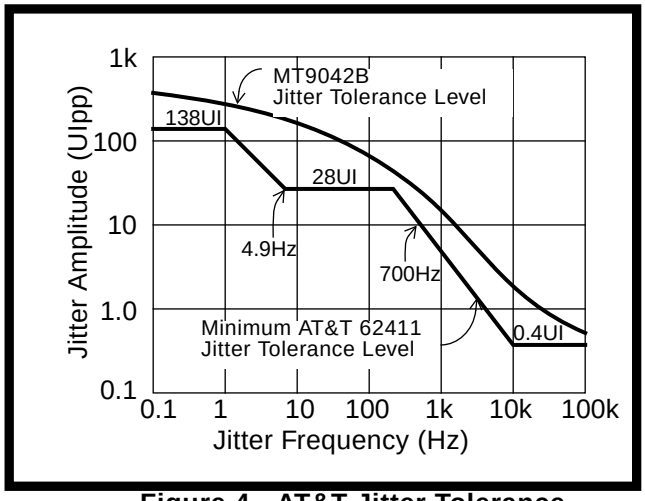

Figure 4 - AT&T Jitter Tolerance

ETSI Jitter Tolerance - the MT9042B meets the ETSI ETS 300 011 jitter tolerance requirements for E1 (2.048MHz) frequency inputs as shown in Figure 5.

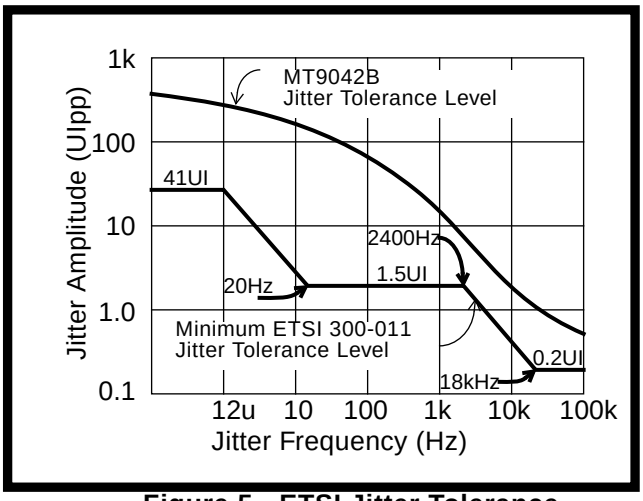

Figure 5 - ETSI Jitter Tolerance

AT&T Jitter Transfer - the MT9042B meets the AT&T TR62411 jitter transfer requirements for T1 (1.544MHz) frequency inputs as shown in Figure 6.

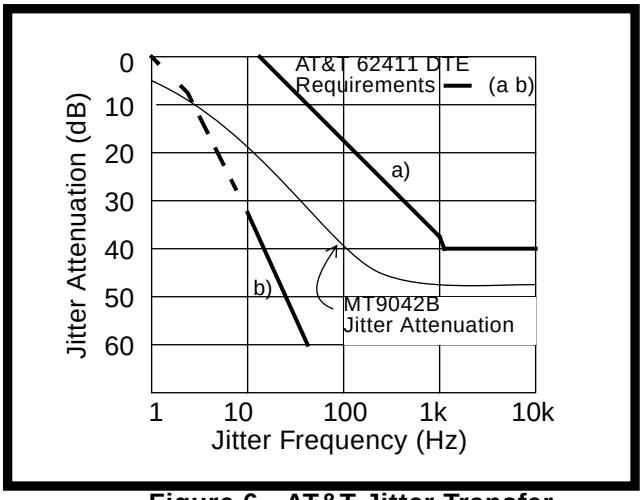

Figure 6 - AT&T Jitter Transfer

ETSI Jitter Transfer - the MT9042B meets all four of the ETSI ETS 300 011 filtered jitter transfer requirements for E1 (2.048MHz) frequency inputs, including the multiple access requirement shown in Figure 7. Note that unlike the AT&T requirement, which specifies an acceptable jitter attenuation range, ETSI specifies a maximum allowable output jitter level, after passing through a bandpass filter for a given input signal level. Although ETSI specifies four different jitter transfer test conditions, the multiple access with 40Hz to 100kHz filter test condition shown in Figure 7 is the most difficult to meet.

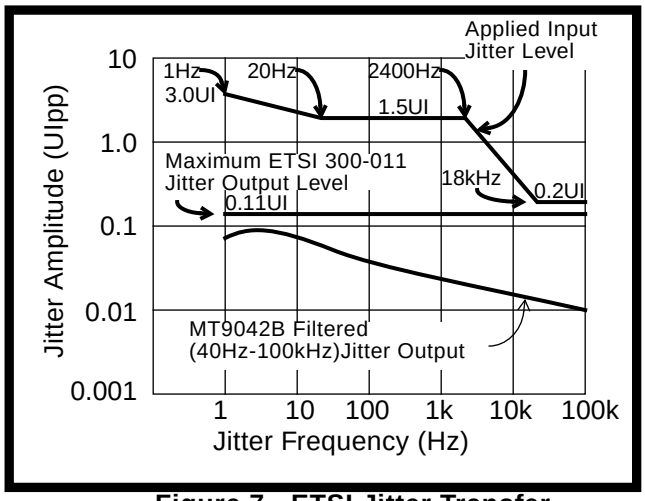

Figure 7 - ETSI Jitter Transfer

ITU-T Jitter Transfer - the MT9042B meets the ITU-T I.431 jitter transfer requirements for E1 (2.048MHz) frequency inputs as shown in Figure 8.

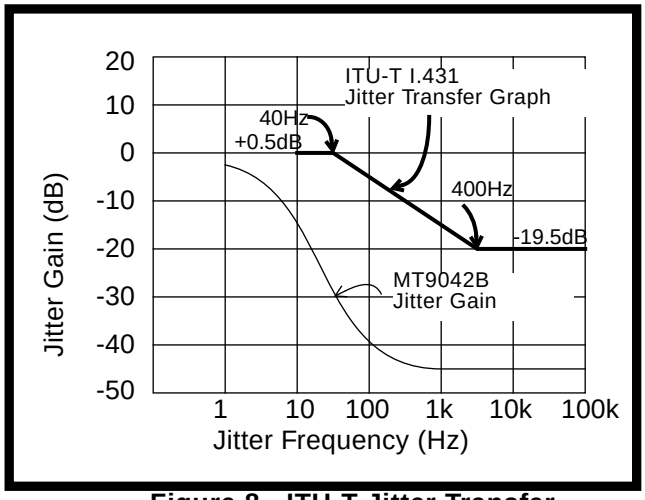

Figure 8 - ITU-T Jitter Transfer

AT&T Frequency Accuracy - the MT9042B meets the AT&T TR62411 output frequency accuracy requirements for all outputs (including 1.544MHz) as shown in Table 3. The MT9042B freerun accuracy is equal to the accuracy of the master clock (OSCi). So if a 32ppm output clock is required, the master clock must also be 32ppm or better

Stratum Level	AT&T Requirement (maximum)	*MT9042B (maximum)
3	4.6ppm	4ppm
4	32ppm	30ppm
4 Enhanced	32ppm	30ppm
* 4ppm with OSCi at 4ppm. * 30ppm with OSCi at 30ppm.		

Table 3 - AT&T Clock Accuracy

ETSI Frequency Accuracy - the MT9042B meets the ETSI ETS 300 011 output frequency accuracy requirements for all outputs (including 2.048MHz) as shown in Table 4. The MT9042B freerun accuracy is equal to the accuracy of the master clock (OSCi). So if a 32ppm output clock is required, the master clock must also be 32ppm or better

ETSI Requirement (maximum)	*MT9042B (maximum)
32ppm	30ppm
* With OSCi at 30ppm.	

Table 4 - ETSI Clock Accuracy

AT&T Holdover Accuracy - the MT9042B meets the AT&T TR62411 holdover requirements as shown in Table 5.

Stratum Level	AT&T Requirement (maximum)	MT9042B (maximum)
3	255 frame slips	35 frame slips
4 Enhanced	Not Required	35 frame slips
4	Not Required	35 frame slips
35 frame slips is equivalent to 0.05ppm.		

Table 5 - AT&T Holdover Accuracy

AT&T Capture Range - the MT9042B meets the AT&T TR62411 capture range (AT&T refers to this as Pull-In Range) for the different stratum levels as shown in Table 6.

Stratum Level	AT&T Requirement (minimum)	*MT9042B (minimum)
3	4.6ppm	226ppm
4 Enhanced	32ppm	200ppm
4	32ppm	200ppm
* 226ppm with OSCi at 4ppm. * 200ppm with OSCi at 30ppm.		

Table 6 - AT&T Capture Range

ETSI Capture Range - the MT9042B meets the ETSI ETS 300 011 capture range as shown in Table 7.

ETSI Requirement (minimum)	*MT9042B (minimum)
32ppm minimum	200ppm
* 200ppm with OSCi at 30ppm.	

Table 7 - ETSI Capture Range

AT&T Phase Slope - the MT9042B meets the AT&T TR62411 phase slope requirements for the different stratum levels as shown in Table 8.

Stratum Level	AT&T Requirement (maximum)	MT9042B (maximum)
3	81ns/1.326ms	53ns/1.326ms
4 Enhanced	81ns/1.326ms	53ns/1.326ms
4	No Requirement	53ns/1.326ms

Table 8 - AT&T Phase Slope

AT&T MTIE - the MT9042B meets the AT&T TR62411 MTIE requirements for the different stratum levels as shown in Table 9.

Stratum Level	AT&T Requirement (maximum)	*MT9042B (maximum)
3	1000ns	200ns/600ns
4 Enhanced	1000ns	200ns/600ns
4	No Requirement	200ns/600ns
*200ns is applicable when the PRI reference and SEC reference are of the same frequency but different in phase. *600ns is applicable when the PRI reference and SEC reference are of different frequencies and measured within 10ms of the input reference change.		

Table 9 - AT&T MTIE

MT9042B Questions and Answers

Common questions relating to the MT9042B, on Holdover Mode, phase slope, MTIE and jitter transfer are answered in the following section.

While in Holdover Mode, how long does it take for 1 complete frame slip?

$$t = \frac{1}{acc \times f}$$

$$t = \frac{1}{0.05 \times 10^{-6} \times 8,000} = 2500s = 42min$$

- *acc = 0.05ppm is the accuracy of Holdover Mode*
- *f = 8,000Hz is the frame frequency*
- *t = 42 minutes is the time for 1 complete frame slip*

While in Holdover Mode, how much does the frame drift in 1.5 seconds?

$$\phi = acc \times t$$

$$\phi = 0.05 \times 10^{-6} \times 1.5 = 75\eta s$$

- *acc = 0.05ppm is the accuracy of Holdover Mode*
- *t = 1.5s is the time duration of the frame drift*
- *ϕ = 75ns is the frame drift or frame phase shift from the ideal position measured in seconds*

While in Holdover Mode, how much does the output signal drift in each frame?

$$\phi = acc \times t = acc \times \frac{1}{f}$$

$$\phi = 0.05 \times 10^{-6} \times \frac{1}{8000} = 7\rho s$$

- *acc = 0.05ppm is the accuracy of Holdover Mode*
- *f = 8,000Hz is the frame frequency*
- *t = 125us is the time duration of the output signal drift*
- *ϕ = 7ps is the output signal drift or phase shift from the ideal position measured in seconds*

While in Holdover Mode, what is the maximum number of frame slips that can occur in 24 hours?

$$Slips = acc \times f \times t$$

$$t = 24hr \times \frac{60min}{1hr} \times \frac{60s}{1min} = 86,400s$$

$$Slips = 0.05 \times 10^{-6} \times 8,000 \times 86,400s = 35$$

- *acc = 0.05ppm is the accuracy of Holdover Mode*
- *f = 8,000Hz is the frame frequency*
- *t = 24hr is the time duration of the frame drift*
- *Slips = 35 is the number of frame slips in 24 hours*

How does jitter and wander on the input reference source affect the holdover accuracy?

Strictly speaking, holdover accuracy does not change with jitter or wander. However, the output of the MT9042B is used as input to the holdover circuitry. Consequently, whatever frequency appears at the output of the MT9042B at the moment Holdover Mode is entered, will be the output holdover frequency. And, this might not be the desired holdover frequency. The instantaneous output frequency of the MT9042B in the presence of jitter or wander is a function of the input reference frequency as well as the applied jitter magnitude and frequency, together with the jitter transfer characteristics of the MT9042B. In general, increases in the deviation of instantaneous output frequency are proportional to increases in input jitter amplitude, increases in jitter frequency which are below the MT9042B loop filter cutoff frequency (1.9Hz), and decreases in jitter frequency which are above the cutoff frequency.

For instance, input jitter of 7.5UIpp at 700Hz at the T1 input is attenuated to 0.020UIpp, which is so small that it has negligible effect on the MT9042B instantaneous output frequency. Consequently, if the device is switched into Holdover Mode with this output signal, the holdover frequency will be within 0.05ppm of the average input frequency.

What is the output holdover frequency when the input reference signal is 1.544MHz with jitter (wander) of 138UIpp at 1Hz?

First we must determine the maximum and minimum input frequency applied to the MT9042B due to the applied jitter (wander). The jittered reference can be described as a frequency modulated signal e(t) as shown below.

$$e(t) = A \cdot \sin((wc \cdot t) + M \cdot \sin(wi \cdot t))$$

- *e(t) = jittered reference signal applied to the MT9042B*
- *A = amplitude of the jittered reference signal*
- *wc = reference carrier frequency (fc=1.544MHz)*
- *t = time*
- *M = modulation index for FM*
- *wi = modulating signal (jitter) frequency (fi=1Hz)*

$$wi = 2 \cdot \pi \cdot fi$$

$$M = \frac{\delta}{fi}$$

- δ*= maximum frequency deviation of the carrier caused by the modulating signal*

$$\delta = jm \cdot \pi \cdot fi$$

$$M = jm \cdot \pi$$

- jm *= peak to peak jitter magnitude (138UIpp)*

Substituting the above yields the following.

$$e(t) = A \cdot \sin((wc \cdot t) + (jm \cdot \pi) \cdot \sin(wi \cdot t))$$

The resulting FM signal generates an infinite number of components (sidebands) spaced at intervals equal to the modulating (jitter) frequency. These components typically lessen in power at frequencies farthest from the carrier. The solution to the FM signal can be found using Bessel Functions. However, since we only want to determine the maximum and minimum frequencies which have significant power, Carsons Rule may be used. Carson's Rule is an approximation which determines the required bandwidth of an FM signal containing about 98% of the total power.

$$BW \cong 2 \cdot (\delta + fi)$$

- BW = Bandwidth of FM signal which contains approximately 98% of the total power

Substituting for δ yields the following.

$$BW \cong 2 \cdot fi \cdot (\pi \cdot jm + 1)$$

$$BW \cong 2 \cdot 1Hz \cdot (\pi \cdot 138UIpp + 1)$$

$$BW \cong 870Hz$$

The corresponding maximum and minimum input frequencies in ppm are determined as follows.

$$\pm\Delta f \cong \left(\frac{BW}{2}\right) \cdot \frac{1}{fc}$$

$$\pm\Delta f \cong \left(\frac{870Hz}{2}\right) \cdot \frac{1}{1.544MHz}$$

$$\pm\Delta f \cong \pm 280ppm$$

- ±Δf = maximum deviation of input reference signal (1.544MHz)

Therefore, the maximum frequency deviation of the jittered 1.544MHz input reference signal is 435Hz (282ppm).

Because the MT9042B uses its output signal as the holdover reference frequency, we must now determine the corresponding output frequency deviation. However, since the applied jitter signal (1Hz) is below the cutoff frequency of the loop filter (1.9Hz), it passes through the device virtually unfiltered (although somewhat slew rate limited).

In conclusion, the worst case holdover output frequency of the MT9042B in the presence of very large magnitude (138UIpp), low frequency (1Hz) jitter, can be as high as 280ppm.

What factors must be considered when determining the MT9042B output phase slope after an input frequency change?

Phase slope is measured in seconds per second and is the rate at which the output signal changes phase with respect to an ideal signal. For the MT9042B, the output signal phase slope is a function of three parameters. This includes the frequency difference between the current frequency and the ideal frequency, the difference in phase between the current phase and the ideal phase, and the elapsed time from the initial signal, state or reference change, to the phase slope measurement interval. The ideal signal is typically equal to the final output signal or final input signal.

Since the difference in phase between the current phase and the ideal phase at the time of the input frequency change is not known, the exact output phase slope cannot be determined. However, the maximum phase slope can be determined,

Two possible cases need to be considered when determining the maximum phase slope. The first case is where there is an input change in phase but the frequency remains the same. In this case, phase correction is done at a maximum rate of 5ns per frame.

$$\frac{d\phi}{dt} = \frac{5\eta s}{125\mu s}$$

- *dϕ is the phase change between the output signal and the "ideal" output signal*
- *dt is the time interval of the phase change measurement (usually 125us or 1.326ms)*

The second case is where there is an input change in frequency. In this case, phase correction is done at a maximum rate of 5ns per frame plus 0.5ps per each additional frame until the output frequency equals the input frequency. The maximum phase slope can be determined as follows.

$$\frac{d\phi}{dt} = \frac{5\eta s}{125\mu s} + N \times \left(\frac{0.5\rho s}{125\mu s}\right)$$

- *N is the number of elapsed frames from the initial frequency change to the measurement interval*

What is the final output phase slope with respect to +24ppm, when the input 8kHz reference frequency changes from +24ppm to -31ppm?

$$df = (24ppm + 31ppm) \times 8,000Hz$$

$$df = 0.44Hz$$

$$\frac{d\phi}{dt} = \frac{df}{f} = \frac{0.44Hz}{8,000Hz} = \frac{55\mu s}{s} = \frac{6.9\eta s}{125us}$$

- *df is the change in frequency*
- *f is the nominal 0ppm 8kHz frequency*

How long will it take the MT9042B to reach the final phase slope value when the input 8kHz reference frequency changes from +24ppm to -31ppm?

Lock time is a function of numerous parameters, one of them being the exact input to output phase delay at the time of the frequency change. Since this is an unknown, an exact lock time cannot be determined. However, a maximum lock time is provided in the

data sheet (30s), and a minimum lock time can be determined as follows.

$$\frac{d\phi}{dt} = \frac{5\eta s}{125\mu s} + N \times \left(\frac{0.5\rho s}{125\mu s}\right)$$

$$T = \left(\frac{-5\eta s}{125\mu s} + \frac{d\phi}{dt}\right) \times \left(\frac{125\mu s}{0.5\rho s}\right)$$

$$T = \left(\frac{-5\eta s}{125\mu s} + \frac{6.9\eta s}{125\mu s}\right) \times \left(\frac{125\mu s}{0.5\rho s}\right)$$

$$N = 3800$$

$$T = 3800 \times 125\mu s = 475ms$$

- *T is the minimum total elapsed time from the initial frequency change to the phase slope measurement interval*

What is the maximum output phase slope with respect to +24ppm, 10ms after the input 8kHz reference frequency changes from +24ppm to -31ppm?

$$N = \frac{10ms}{125us} = 80$$

$$\frac{d\phi}{dt} = \frac{5\eta s}{125\mu s} + 80 \times \left(\frac{0.5\rho s}{125\mu s}\right)$$

$$\frac{d\phi}{dt} = \frac{5.04\eta s}{125\mu s}$$

Note that after 10ms, regardless of the size of the input phase or frequency step, the output phase slope will not be larger than 5.04ns per frame. This meets the Accunet TR62411 specification for maximum phase slope of 7.6ns/125us (81ns/1.326ms).

What is the resulting maximum MTIE if the input signal changes from +24ppm to -31ppm, and 10ms later a reference switch is made to a new +24ppm signal?

$$MTIE = PC + \Delta\phi$$

$$\Delta\phi = \frac{d\phi}{dt} \times T$$

$$PC = 200ns$$

$$T = 10ms$$

$$\Delta\phi = \frac{5.04\eta s}{125\mu s} \times 10ms = 403ns$$

$$MTIE = 200ns + 403ns = 603ns$$

- *PC is the MT9042B phase continuity (see data sheet) when switching between references*
- *$\Delta\phi$ is the phase change between the output signal and the "ideal" output signal after the elapsed time of T*

Note that after 10ms, regardless of the size of the input phase or frequency step, the maximum output phase slope will not be larger than 5.04ns per frame. And consequently, MTIE will not exceed 600ns, providing reference switching is done within 10ms of the initial input disturbance. This meets the Accunet TR62411 specification for maximum phase slope of 7.6ns/125us (81ns/1.326ms) and MTIE of 1000ns.

Does the MT9042B meet the AT&T 62411 jitter transfer requirements for an 8kHz input signal?

There are no jitter transfer requirements listed in AT&T 62411 for an 8kHz input signal. AT&T specify applied jitter values in the range of 1Hz to 10kHz for a 1.544MHz signal.

With an 8kHz signal, jitter frequencies higher than one half of 8kHz will be aliased down to a lower frequency before they are input to the PLL. In other words, you cannot create an 8kHz signal with 10kHz of jitter on it. It will in fact be an 8kHz signal with 2kHz of jitter.

This is why unexpected results may occur when using a 1.544MHz clock extractor followed by a 193 divider to provide an 8kHz clock source. For instance, if 8001Hz jitter is applied to the 1.544MHz signal, and this is followed by a divide by 193 circuit, the resulting output will be 8kHz with 1Hz jitter. Any synchronizer or PLL following this arrangement will "see" an 8KHz signal with 1Hz jitter because that is what is really there. And the device will attenuate the 1Hz jitter according to its internal transfer function. In most cases, 1Hz is not attenuated. And consequently, the amplitude of the 8001Hz jitter signal applied to the divide by 193 circuit is passed unattenuated through the divide circuit and through the PLL.

For example, if a 1.544MHz signal with 0.5UIpp 8001Hz jitter is applied to a clock extractor, and if the clock extractor provides no jitter attenuation, and is followed by a divide by 193 circuit, then the output of the divider will be 8kHz with 0.5UIpp 1Hz jitter. If this signal is input to the MT9042B which has a low pass cutoff frequency of 1.9Hz, then the 0.5UIpp 1Hz jitter will pass through the device virtually unattenuated.

This may or may not be a problem for the system, but what should be noted are the effects of using this method.

References

"MT9042B Multitrunk System Synchronizer" Data Sheet, Mitel Semiconductor, Issue 1, October 1996.

AT&T TR62411 "Accunet® T1.5 Service Description and Interface Specification", December 1990.

ANSI T1.101-1994 "Synchronization Interface Standard", February 1994.

ETSI 300 011:1992 "ISDN; Primary rate user-network interface Layer 1 specification and test principles", April 1992.

ITU-T Recommendation I.431 "Primary Rate User-Network Interface - Layer 1 Specification", March 1993.

Application Circuits

This section contains MT9042B application specific details for extending the number of reference inputs from two to four.

Four Reference Sources with MT9042B in 8kHz Manual Control

This application circuit (Figure 19) shows one method of multiplexing in four external reference sources into the MT9042B while maintaining phase continuity at its output during reference switching.

MUX1 provides one of four reference signals to the MT9042B primary input. MUX2 provides one of four reference signals to the MT9042B secondary input. To ensure that no phase step occurs at the output of the MT9042B during reference switching, only the MUX that is not providing the current reference source may be switched. After the MUX switch is established, then the MT9042B switch using RSEL can occur. This ensures that phase continuity is always maintained.

Consider the following example. The MT9042B is initially operating off of the PRI input with 3-E8K (Line 3) through MUX 1. SEC is connected through MUX2 to 2-E8K (Line 2). A fault condition occurs on Line 3, a loss of signal indication (3-L) is provided to the controller which puts the MT9042B into Holdover Mode, the controller then begins to initiate the reference switch. Since the MUX (MUX2) that is not providing the current reference is already established, RSEL of the MT9042B is changed from logic 0 to logic 1. This performs the reference switch within the MT9042B, so phase continuity is maintained. The new reference is now Line 2.

The controller can now setup MUX1 and PRI with a good reference source (Line 1 or Line 4) in the event Line 2 goes bad.

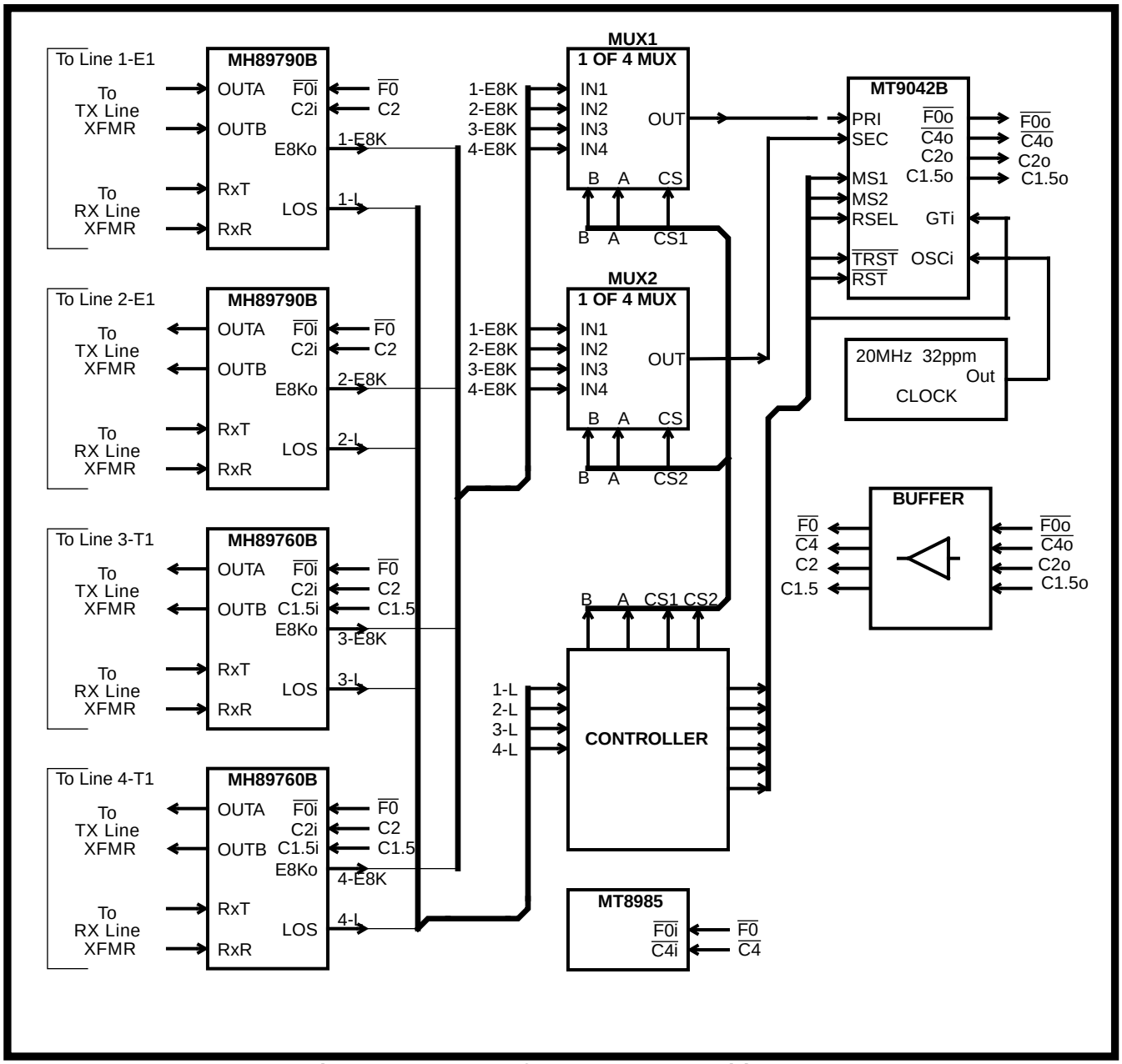

Figure 19 - Four Reference Sources with MT9042B

Notes: